Features

- High-performance, low-power Atmel®AVR®XMEGA® 8/16-bit Microcontroller
- Nonvolatile program and data memories
  - 256KBytes of in-system self-programmable flash
  - 8KBytes boot section
  - 4KBytes EEPROM
  - 16KBytes internal SRAM
- Peripheral features
  - Four-channel DMA controller
  - Eight-channel event system
  - Seven 16-bit timer/counters
    - Four timer/counters with four output compare or input capture channels
    - Three timer/counters with two output compare or input capture channels
    - High resolution extension on all timer/counters
    - Advanced waveform extension (AWeX) on one timer/counter
  - One USB device interface
    - USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant
    - 32 Endpoints with full configuration flexibility
  - Six USARTs with IrDA support for one USART
  - Two two-wire interfaces with dual address match (I^2C and SMBus compatible)
  - Two serial peripheral interfaces (SPIs)
  - AES and DES crypto engine
  - CRC-16 (CRC-CCITT) and CRC-32 (IEEE® 802.3) generator
  - 32-bit real time counter (RTC) with separate oscillator and battery backup system
  - Two sixteen-channel, 12-bit, 2msps Analog to Digital Converters
  - One two-channel, 12-bit, 1msps Digital to Analog Converter
  - Four Analog Comparators with window compare function, and current sources
  - External interrupts on all general purpose I/O pins
  - Programmable watchdog timer with separate on-chip ultra low power oscillator
  - QTouch® library support
    - Capacitive touch buttons, sliders and wheels
- Special microcontroller features
  - Power-on reset and programmable brown-out detection
  - Internal and external clock options with PLL and prescaler
  - Programmable multilevel interrupt controller
  - Five sleep modes
  - Programming and debug interfaces
    - JTAG (IEEE 1149.1 compliant) interface, including boundary scan
    - PDI (Program and Debug Interface)
- I/O and packages
  - 47 programmable I/O pins
  - 64-lead TQFP
  - 64-pad QFN
- Operating voltage
  - 1.6 – 3.6V
- Operating frequency
  - 0 – 12MHz from 1.6V
  - 0 – 32MHz from 2.7V

Typical Applications

- Industrial control
- Factory automation
- Building control
- Board control
- White goods
- Climate control
- RF and ZigBee®
- USB connectivity
- Networking
- Optical
- Low power battery applications
- Power tools
- HVAC
- Utility metering
- Medical applications

8/16-bit Atmel XMEGA A3BU Microcontroller

ATxmega256A3BU

8362E–AVR–01/12

1. Ordering Information

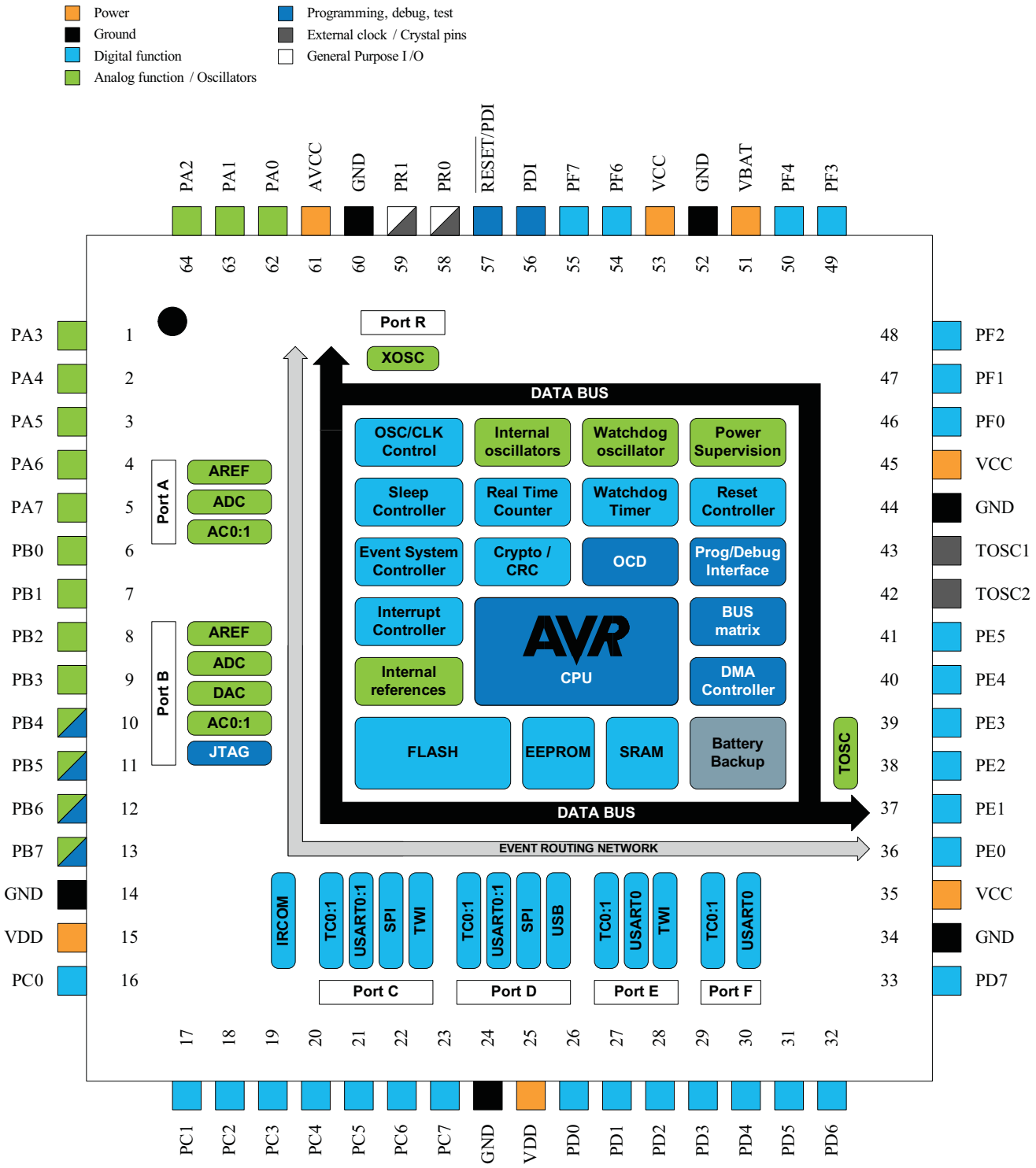
Ordering Code	Flash	EEPROM	SRAM	Speed [MHz]	Power Supply	Package [1][2][3]	Temp
ATxmega256A3BU-AU	256K + 8K	4K	16K	32	1.6 - 3.6V	64A	-40°C - 85°C
ATxmega256A3BU-AUR [4]							
ATxmega256A3BU-MH	256K + 8K	4K	16K	32	1.6 - 3.6V	64M2	
ATxmega256A3BU-MHR [4]							

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see ”Packaging information” on page 70.
4. Tape and reel.

Package Type	
64A	64-lead, 14 x 14mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
64M2	64-pad, 9 x 9 x 1.0mm body, lead pitch 0.50mm, 7.65mm exposed pad, quad flat no-lead package (QFN)

2. Pinout/Block Diagram

Figure 2-1. Block diagram and pinout.



Notes: 1. For full details on pinout and pin functions refer to "Pinout and Pin Functions" on page 59.

2. The large center pad underneath the QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

3. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA device achieves CPU throughput approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA A3BU devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; four-channel DMA controller; eight-channel event system and programmable multilevel interrupt controller; 47 general purpose I/O lines; 32-bit real-time counter (RTC) with battery backup system; seven flexible 16-bit Timer/Counters with compare modes and PWM; one full speed USB 2.0 interface; six USARTs; two two-wire serial interfaces (TWIs); two serial peripheral interfaces (SPIs); AES and DES cryptographic engine; two 16-channel, 12-bit ADCs with programmable gain; one 2-channel 12-bit DAC; four analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available. The devices also have an IEEE std. 1149.1 compliant JTAG interface, and this can also be used for boundary scan, on-chip debug and programming.

The XMEGA A3BU devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, DMA controller, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, USB resume, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

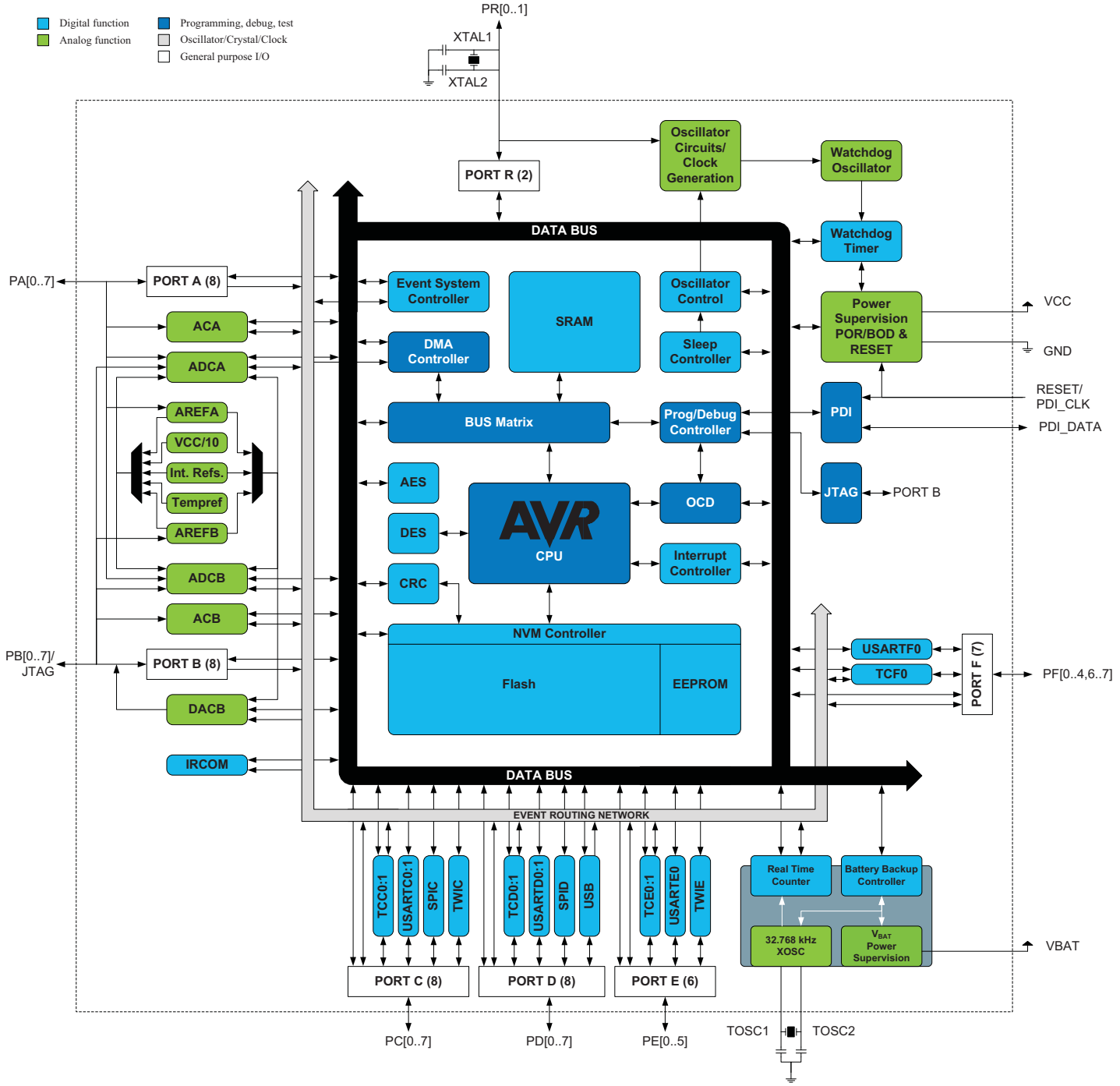
Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI or JTAG interfaces. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All Atmel AVR XMEGA devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

3.1 Block Diagram

Figure 3-1. XMEGA A3BU block diagram.



15. Interrupts and Programmable Multilevel Interrupt Controller

15.1 Features

- **Short and predictable interrupt response time**
- **Separate interrupt configuration and vector address for each interrupt**
- **Programmable multilevel interrupt controller**
  - **Interrupt prioritizing according to level and vector address**
  - **Three selectable interrupt levels for all interrupts: low, medium and high**
  - **Selectable, round-robin priority scheme within low-level interrupts**
  - **Non-maskable interrupts for critical functions**
- **Interrupt vectors optionally placed in the application section or the boot loader section**

15.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

15.3 Interrupt vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA A3BU devices are shown in Table 15-1. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA AU manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 15-1. The program address is the word address.

Table 15-1. Reset and interrupt vectors.

Program address (base address)	Source	Interrupt description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal oscillator failure interrupt vector (NMI)
0x004	PORTC_INT_base	Port C interrupt base
0x008	PORTR_INT_base	Port R interrupt base
0x00C	DMA_INT_base	DMA controller interrupt base

Table 15-1. Reset and interrupt vectors. (Continued)

Program address (base address)	Source	Interrupt description
0x014	RTC32_INT_base	32-bit Real Time Counter interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C interrupt base
0x01C	TCC0_INT_base	Timer/Counter 0 on Port C interrupt base
0x028	TCC1_INT_base	Timer/Counter 1 on Port C interrupt base
0x030	SPIC_INT_vect	SPI on Port C interrupt vector
0x032	USARTC0_INT_base	USART 0 on Port C interrupt base
0x038	USARTC1_INT_base	USART 1 on Port C interrupt base
0x03E	AES_INT_vect	AES interrupt vector
0x040	NVM_INT_base	Non-Volatile Memory interrupt base
0x044	PORTB_INT_base	Port B interrupt base
0x048	ACB_INT_base	Analog Comparator on Port B interrupt base
0x04E	ADCB_INT_base	Analog to Digital Converter on Port B interrupt base
0x056	PORTE_INT_base	Port E interrupt base
0x05A	TWIE_INT_base	Two-Wire Interface on Port E interrupt base
0x05E	TCE0_INT_base	Timer/Counter 0 on Port E interrupt base
0x06A	TCE1_INT_base	Timer/Counter 1 on Port E interrupt base
0x074	USARTE0_INT_base	USART 0 on Port E interrupt base
0x080	PORTD_INT_base	Port D interrupt base
0x084	PORTA_INT_base	Port A interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A interrupt base
0x09A	TCD0_INT_base	Timer/Counter 0 on Port D interrupt base
0x0A6	TCD1_INT_base	Timer/Counter 1 on Port D interrupt base
0x0AE	SPID_INT_vector	SPI on Port D interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on Port D interrupt base
0x0B6	USARTD1_INT_base	USART 1 on Port D interrupt base
0x0D0	PORTF_INT_base	Port F interrupt base
0x0D8	TCF0_INT_base	Timer/Counter 0 on Port F interrupt base
0x0EE	USARTF0_INT_base	USART 0 on Port F interrupt base
0x0FA	USB_INT_base	USB on Port D interrupt base

33. Pinout and Pin Functions

The device pinout is shown in ”Pinout/Block Diagram” on page 3. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

33.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

33.1.1 Operation/Power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
VBAT	Battery Backup Module supply voltage
GND	Ground

33.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

33.1.3 Analog functions

ACn	Analog Comparator input pin n
ACnOUT	Analog Comparator n Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
A_{REF}	Analog Reference input pin

33.1.4 Timer/Counter and AWEX functions

OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

33.1.5 Communication functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled
XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
$\overline{SS}$	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI
D-	Data- for USB
D+	Data+ for USB

33.1.6 Oscillators, Clock and Event

TOSCn	Timer Oscillator pin n
XTALn	Input/Output for Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel Output
RTCOUT	RTC Clock Source Output

33.1.7 Debug/System functions

$\overline{RESET}$	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin
TCK	JTAG Test Clock
TDI	JTAG Test Data In
TDO	JTAG Test Data Out
TMS	JTAG Test Mode Select

33.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

Table 33-1. Port A - alternate functions.

PORT A	PIN #	INTERRUPT	ADCA POS/GAINPOS	ADCB POS	ADCA NEG	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	REFA
GND	60									
AV_{CC}	61									
PA0	62	SYNC	ADC0	ADC8	ADC0		AC0	AC0		AREF
PA1	63	SYNC	ADC1	ADC9	ADC1		AC1	AC1		
PA2	64	SYNC/ASYNC	ADC2	ADC10	ADC2		AC2			
PA3	1	SYNC	ADC3	ADC11	ADC3		AC3	AC3		
PA4	2	SYNC	ADC4	ADC12		ADC4	AC4			
PA5	3	SYNC	ADC5	ADC13		ADC5	AC5	AC5		
PA6	4	SYNC	ADC6	ADC14		ADC6	AC6		AC1OUT	
PA7	5	SYNC	ADC7	ADC15		ADC7		AC7	AC0OUT	

Table 33-2. Port B - alternate functions.

PORT B	PIN #	INTERRUPT	ADCA POS	ADCB POS/GAINPOS	ADCB NEG	ADCB GAINNEG	ACB POS	ACB NEG	ACB OUT	DACB	REFB	JTAG
PB0	6	SYNC	ADC8	ADC0	ADC0		AC0	AC0			AREF	
PB1	7	SYNC	ADC9	ADC1	ADC1		AC1	AC1				
PB2	8	SYNC/ASYNC	ADC10	ADC2	ADC2		AC2			DAC0		
PB3	9	SYNC	ADC11	ADC3	ADC3		AC3	AC3		DAC1		
PB4	10	SYNC	ADC12	ADC4		ADC4	AC4					TMS
PB5	11	SYNC	ADC13	ADC5		ADC5	AC5	AC5				TDI
PB6	12	SYNC	ADC14	ADC6		ADC6	AC6		AC1OUT			TCK
PB7	13	SYNC	ADC15	ADC7		ADC7		AC7	AC0OUT			TDO
GND	14											
V_{CC}	15											

Table 33-3. Port C - alternate functions.

PORT C	PIN #	INTERRUPT	TCC0 [1][2]	AWEXC	TCC1	USARTC0 [3]	USARTC1	SPIC [4]	TWIC	CLOCKOUT [5]	EVENTOUT [6]
PC0	16	SYNC	OC0A	OC0ALS					SDA		
PC1	17	SYNC	OC0B	OC0AHS		XCK0			SCL		
PC2	18	SYNC/ASYNC	OC0C	OC0BLS		RXD0					
PC3	19	SYNC	OC0D	OC0BHS		TXD0					
PC4	20	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PC5	21	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PC6	22	SYNC		OC0DLS			RXD1	MISO		clk_{RTC}	
PC7	23	SYNC		OC0DHS			TXD1	SCK		clk_{PER}	EVOUT
GND	24										
V_{CC}	25										

Notes:
1. Pin mapping of all TC0 can optionally be moved to high nibble of port.
2. If TC0 is configured as TC2 all eight pins can be used for PWM output.
3. Pin mapping of all USART0 can optionally be moved to high nibble of port.
4. Pins MOSI and SCK for all SPI can optionally be swapped.
5. CLKOUT can optionally be moved between port C, D and E and between pin 4 and 7.
6. EVOUT can optionally be moved between port C, D and E and between pin 4 and 7.

Table 33-4. Port D - alternate functions.

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USBD	USARTD0	USARTD1	SPID	TWID	CLOCKOUT	EVENTOUT
PD0	26	SYNC	OC0A						SDA		
PD1	27	SYNC	OC0B			XCK0			SCL		
PD2	28	SYNC/ASYNC	OC0C			RXD0					
PD3	29	SYNC	OC0D			TXD0					
PD4	30	SYNC		OC1A				$\overline{SS}$			
PD5	31	SYNC		OC1B			XCK1	MOSI			
PD6	32	SYNC			D-		RXD1	MISO			
PD7	33	SYNC			D+		TXD1	SCK		clk_{PER}	EVOUT
GND	34										
V_{CC}	35										

Table 33-5. Port E - alternate functions.

PORT E	PIN #	INTERRUPT	TCE0	TCE1	USARTE0	TWIE
PE0	36	SYNC	OC0A			SDA
PE1	37	SYNC	OC0B		XCK0	SCL
PE2	38	SYNC/ASYNC	OC0C		RXD0	
PE3	39	SYNC	OC0D		TXD0	
PE4	40	SYNC		OC1A		
PE5	41	SYNC		OC1B		
TOSC2	42					
TOSC1	43					
GND	44					
V_{CC}	45					

Table 33-6. Port F - alternate functions.

PORT F	PIN #	INTERRUPT	TCF0	USARTF0
PF0	46	SYNC	OC0A	
PF1	47	SYNC	OC0B	XCK0
PF2	48	SYNC/ASYNC	OC0C	RXD0
PF3	49	SYNC	OC0D	TXD0
PF4	50	SYNC		
VBAT	51			
GND	52	SYNC		
VCC	53	SYNC		
PF6	54			
PF7	55			

Table 33-7. Port R - alternate functions.

PORT R	PIN #	INTERRUPT	PDI	XTAL
PDI	56		PDI_DATA	
$\overline{\text{RESET}}$	57		PDI_CLOCK	
PR0	58	SYNC		XTAL2
PR1	59	SYNC		XTAL1

34. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in Atmel AVR XMEGA A3BU. For complete register description and summary for each peripheral module, refer to the XMEGA AU Manual.

Base Address	Name	Description
0x0000	GPIO	General purpose IO registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock Control
0x0048	SLEEP	Sleep Controller
0x0050	OSC	Oscillator Control
0x0060	DFLLRC32M	DFLL for the 32MHz internal oscillator
0x0068	DFLLRC2M	DFLL for the 2MHz internal oscillator
0x0070	PR	Power Reduction
0x0078	RST	Reset Controller
0x0080	WDT	Watch-Dog Timer
0x0090	MCU	MCU Control
0x00A0	PMIC	Programmable Multilevel Interrupt Controller
0x00B0	PORTCFG	Port Configuration
0x00C0	AES	AES module
0x00D0	CRC	CRC generator
0x00F0	VBAT	VBAT Battery Backup module
0x0100	DMA	DMA Controller
0x0180	EVSYS	Event System
0x01C0	NVM	Non Volatile Memory (NVM) Controller
0x0200	ADCA	Analog to Digital Converter on port A
0x0240	ADCB	Analog to Digital Converter on port B
0x0320	DACB	Digital to Analog Converter on port B
0x0380	ACA	Analog Comparator pair on port A
0x0390	ACB	Analog Comparator pair on port B
0x0420	RTC32	32-bit Real Time Counter
0x0480	TWIC	Two-wire Interface on port C
0x04A0	TWIE	Two-wire Interface on port E
0x04D0	USBD	USB Device
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C
0x0660	PORTD	Port D
0x0680	PORTE	Port E
0x06A0	PORTF	Port F
0x07E0	PORTR	Port R
0x0800	TCC0	Timer/Counter 0 on port C
0x0840	TCC1	Timer/Counter 1 on port C
0x0880	AWEXC	Advanced Waveform Extension on port C
0x0890	HIRESC	High Resolution Extension on port C
0x08A0	USARTC0	USART 0 on port C
0x08B0	USARTC1	USART 1 on port C
0x08C0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0900	TCD0	Timer/Counter 0 on port D
0x0940	TCD1	Timer/Counter 1 on port D
0x0990	HIRESD	High Resolution Extension on port D
0x09A0	USARTD0	USART 0 on port D
0x09B0	USARTD1	USART 1 on port D
0x09C0	SPID	Serial Peripheral Interface on port D
0x0A00	TCE0	Timer/Counter 0 on port E
0x0A40	TCE1	Timer/Counter 1 on port E
0x0A80	AWEXE	Advanced Waveform Extension on port E
0x0A90	HIRESE	High Resolution Extension on port E
0x0AA0	USARTE0	USART 0 on port E
0x0B00	TCF0	Timer/Counter 0 on port F
0x0B90	HIRESF	High Resolution Extension on port F

Base Address	Name	Description
0x0BA0	USARTF0	USART 0 on port F

35. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	Rd ← Rd + 1:Rd + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	Rd ← Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd ← Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd ← Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd - K - C	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	Rd + 1:Rd ← Rd + 1:Rd - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One's Complement	Rd ← $FF - Rd	Z,C,N,V,S	1
NEG	Rd	Two's Complement	Rd ← $00 - Rd	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd ← Rd - 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd ← $FF	None	1
MUL	Rd,Rr	Multiply Unsigned	R1:R0 ← Rd x Rr (UU)	Z,C	2
MULS	Rd,Rr	Multiply Signed	R1:R0 ← Rd x Rr (SS)	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr (SU)	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	R1:R0 ← Rd x Rr<<1 (UU)	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	R1:R0 ← Rd x Rr<<1 (SS)	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← Rd x Rr<<1 (SU)	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 ← Encrypt(R15:R0, K) else if (H = 1) then R15:R0 ← Decrypt(R15:R0, K)		1 / 2
Branch instructions					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2
EIJMP		Extended Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	2
JMP	k	Jump	PC ← k	None	3
RCALL	k	Relative Call Subroutine	PC ← PC + k + 1	None	2 / 3 (1)
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3 (1)
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3 (1)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CALL	k	call Subroutine	PC ← k	None	3 / 4 (1)
RET		Subroutine Return	PC ← STACK	None	4 / 5 (1)
RETI		Interrupt Return	PC ← STACK	I	4 / 5 (1)
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data transfer instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2 (1)(2)
LD	Rd, X	Load Indirect	Rd ← (X)	None	1 (1)(2)
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1 (1)(2)
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2 (1)(2)
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1 (1)(2)
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1 (1)(2)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y ← Y - 1 Rd ← (Y)	None	2 (1)(2)
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2 (1)(2)
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1 (1)(2)
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	1 (1)(2)
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2 (1)(2)
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2 (1)(2)
STS	k, Rr	Store Direct to Data Space	(k) ← Rd	None	2 (1)
ST	X, Rr	Store Indirect	(X) ← Rr	None	1 (1)
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1 (1)
ST	-X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2 (1)
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1 (1)
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1 (1)
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2 (1)
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2 (1)
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1 (1)
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) ← Rr Z ← Z + 1	None	1 (1)
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1	None	2 (1)
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2 (1)
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd ← (Z), Z ← Z + 1	None	3
ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3
ELPM	Rd, Z	Extended Load Program Memory	Rd ← (RAMPZ:Z)	None	3
ELPM	Rd, Z+	Extended Load Program Memory and Post-Increment	Rd ← (RAMPZ:Z), Z ← Z + 1	None	3
SPM		Store Program Memory	(RAMPZ:Z) ← R1:R0	None	-
SPM	Z+	Store Program Memory and Post-Increment by 2	(RAMPZ:Z) ← R1:R0, Z ← Z + 2	None	-
IN	Rd, A	In From I/O Location	Rd ← I/O(A)	None	1
OUT	A, Rr	Out To I/O Location	I/O(A) ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	1 (1)
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2 (1)
XCH	Z, Rd	Exchange RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp	None	2
LAS	Z, Rd	Load and Set RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp v (Z)	None	2
LAC	Z, Rd	Load and Clear RAM location	Temp ← Rd, Rd ← (Z), (Z) ← ($FFh – Rd) • (Z)	None	2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
LAT	Z, Rd	Load and Toggle RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp ⊕ (Z)	None	2
Bit and bit-test instructions					
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0, C ← Rd(7)	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0, C ← Rd(0)	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ↔ Rd(7..4)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	I/O(A, b) ← 1	None	1
CBI	A, b	Clear Bit in I/O Register	I/O(A, b) ← 0	None	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two's Complement Overflow	V ← 1	V	1
CLV		Clear Two's Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU control instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes: 1. Cycle times for Data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
2. One extra cycle must be added when accessing Internal SRAM.